

A METHOD FOR ERASING AN NROM CELL

TECHNICAL FIELD OF THE INVENTION

[0001] The present invention relates generally to memory devices and in particular the present invention relates to erasing nitride read only memory cells.

BACKGROUND OF THE INVENTION

[0002] Memory devices are typically provided as internal storage areas in the computer. The term memory identifies data storage that comes in the form of integrated circuit chips. In general, memory devices contain an array of memory cells for storing data, and row and column decoder circuits coupled to the array of memory cells for accessing the array of memory cells in response to an external address.

[0003] There are several different types of memory such as random access memory (RAM) and read only memory (ROM). RAM is typically used as main memory in a computer environment. One can repeatedly read data from and write data into RAM. Most RAM is volatile, which means that it requires a steady flow of electricity to maintain its contents. When the power is turned off, the data in RAM is lost.

[0004] This is in contrast to ROM that generally only permits the user to read data already stored in the ROM but the ROM retains data after power is removed (i.e., non-volatile). Computers almost always contain a small amount of ROM that holds instructions for starting up the computer. Unlike RAM, ROM generally cannot be written to in routine operation.

[0005] Another type of non-volatile memory is flash memory. A flash memory is a type of EEPROM that can be erased and reprogrammed in blocks instead of one byte at a time. Many modern PCs have their BIOS stored on a flash memory chip so that it can easily be updated if necessary. Flash memory is also popular in modems because it enables the modem manufacturer to support new protocols as they become standardized.

[0006] Yet another type of non-volatile memory is a nitride read only memory (NROM). NROM has some of the characteristics of flash memory but does not require the

special fabrication processes of flash memory. NROM can be implemented using a standard CMOS process.

[0007] Because of NROM's compatibility with the CMOS process, a short-channel NROM memory can be embedded into other architectures, such as microcontrollers, that also use the CMOS process. One possible type of embedded memory uses short channel NROM cells with single bit/cell storage. In this type of memory, the effective bit size is larger than in standard NROM cells with double bit/cell but the voltages used for programming/erasing are all consistent with the CMOS host process. However, one problem with embedding the short-channel NROM is that the NROM cells are sensitive to over-erasure.

[0008] For the reasons stated above, and for other reasons stated below which will become apparent to those skilled in the art upon reading and understanding the present specification, there is a need in the art for a way to erase NROM arrays without being over-erased.

SUMMARY

[0009] The above-mentioned problems with erasing NROM arrays and other problems are addressed by the present invention and will be understood by reading and studying the following specification.

[0010] The various embodiments relate to erasing NROM blocks of memory that comprise a plurality of memory cells. Each cell has a gate input and two source/drain regions. The method comprises erasing the memory block and performing a recovery operation on the plurality of memory cells such that a voltage threshold for over-erased cells is increased.

[0011] In another embodiment, the method erases the memory block and then performs a verification operation on the cells. If a read operation does not produce a column current, the erase operation was successful. If the read operation produces a column current, the recovery operation is performed to increase the threshold voltage. The verification is

repeated until the column current is not detected indicating that the overerased cells are recovered.

[0012] Further embodiments of the invention include methods and apparatus of varying scope.

BRIEF DESCRIPTION OF THE DRAWINGS

[0013] Figures 1A and 1B show diagrams of an NROM memory cell of the present invention.

[0014] Figure 2 shows a flow chart of a method for erasing an NROM memory cell in accordance with one embodiment of the present invention.

[0015] Figure 3 shows a flow chart of a method for erasing an NROM memory cell in accordance with an alternate embodiment of the present invention.

[0016] Figure 4 shows a block diagram of one embodiment of an electronic system of the present invention having an embedded NROM array.

DETAILED DESCRIPTION

[0017] In the following detailed description of the invention, reference is made to the accompanying drawings that form a part hereof, and in which is shown, by way of illustration, specific embodiments in which the invention may be practiced. In the drawings, like numerals describe substantially similar components throughout the several views. These embodiments are described in sufficient detail to enable those skilled in the art to practice the invention. Other embodiments may be utilized and structural, logical, and electrical changes may be made without departing from the scope of the present invention. The following detailed description is, therefore, not to be taken in a limiting sense, and the scope of the present invention is defined only by the appended claims and equivalents thereof.

[0018] Figures 1A and 1B illustrate NROM memory cells of the present invention. This cell is comprised of a control gate 100 formed on top of an oxide layer 101. Below the

oxide layer is a layer of nitride 103 upon which the charge is stored for the various states of the cell. In one embodiment, the cell has areas 105 and 106 for storing two bits of data on the nitride 103. The nitride layer 103 can be patterned in small pieces matching the size of each individual NROM cell (Figure 1A) or in large sheets to uniformly cover the area of each memory array block (Figure 1B).

[0019] Two source/drain regions 109 and 111 are at either end of the gate layer 101. The source/drain regions 109 and 111 are connected by a channel area 110 between the two regions 109 and 111. The function of each source/drain region 109 or 111 (i.e., whether source or drain) depends upon which bit area 105 or 106 is being read or written. For example, if the carrier is input at the left side source/drain region 111 and output from the right side region 109 in a read operation, the left side is the source 111 and the right side is the drain 109 and the data bit charge is stored on the nitride 103 at the source end 111.

[0020] An NROM memory block is comprised of a large number of the cells of Figure 1. The present invention is not limited to any one quantity of NROM cells that comprise a memory block. Especially in an embedded embodiment, the quantity of cells comprising a block depends on the memory requirements of the circuitry into which the NROM cells are embedded.

[0021] Standard long-channel NROM cells for double-bit storage are inherently insensitive to over-erasure. The threshold voltage for such a cell in an erased state is kept at its “neutral” value by the mid-channel region away from either source/drain region, which has no holes trapped in the nitride dielectric above.

[0022] A newer type of short-channel NROM cells forgoes the double-bit storage in exchange for programming at a lower voltage. Such cell structure and operation are particularly well suited for embedded memory applications. These short-channel (i.e., < 0.2 microns) NROM cells can inject hot holes in the mid-channel region during an erase operation and thus become sensitive to over-erasure like traditional stack-gate flash memory. The NROM cell erase methods of the present invention operate best with short

channel (single-bit) architectures. However, the methods may be adapted to work with other types of NROM cell architecture.

[0023] Figure 2 illustrates a flow chart of a method for erasing an NROM memory array in accordance with one embodiment of the present invention. This method first erases an NROM memory block 201 as is well known in the art. This is accomplished, in one embodiment by coupling one source/drain region to a voltage in the range of 3 to 8V. The gate connection is coupled to a voltage in the range of -12 to 0V. The remaining source/drain region is coupled to a voltage in the range of 3 to 8V. In an alternate embodiment, the other source/drain connection is grounded or floating. This embodiment assumes that the voltages above are applied simultaneously to all NROM cells of a memory block for a duration long enough so that the NROM memory block is properly erased.

[0024] A high efficiency recovery operation is then performed 203. This operation raises the threshold voltage, V_t , for any over-erased cells. As is well known in the art, each cell has a threshold voltage that indicates when the cell is either programmed or erased. In one embodiment, cells with threshold voltages equal to or greater than a certain boundary (e.g., $V_t = 4V$) are considered to be programmed while threshold voltages less than the same boundary value are considered erased. Alternate embodiments may use different states. On the other hand, when the threshold voltage of an erased cell is lower than another boundary value (e.g., $V_t = 0V$), the cell is considered to be over-erased as it may induce column current when it is not selected in a read operation. The recovery step 203 is meant to raise the threshold voltage for all over-erased cells above the boundary for over-erasure (e.g., $V_t = 0V$), while keeping all cells in erased state (e.g., $V_t < 4V$).

[0025] In the recovery step 203, all of the cells in the memory block are biased at certain voltage ranges with the gate connection being coupled to a ramped voltage. In one embodiment, the source/drain region acting as a drain is coupled to a constant voltage in the range of 3 to 7V. The source/drain region acting as a source is coupled to a constant voltage in the range of 0 to 3V. In an alternate embodiment, this connection may be left floating. The gate connection is coupled to a ramped voltage in which the initial voltage is

in the range of -3 to 0V and the final voltage is in the range of 1 to 3V. The ramp occurs in a time period of from 10 μ s to 1 second.

[0026] Alternate embodiments use other voltage for the source/drain regions and other initial and final voltages for the ramped gate voltage. Additionally, the present invention is not limited to any one time period over which the ramped voltage occurs.

[0027] Figure 3 illustrates a flow chart of a method for erasing an NROM memory block in accordance with an alternate embodiment of the present invention. As in the prior embodiment, the NROM memory block is first erased 301 as is known in the art. This can be accomplished using the voltages as described above or by using other voltages.

[0028] In this embodiment, an erase verify operation can be performed 303 to verify complete erasure of the memory block. If, at this step, the block is found not completely erased, the algorithm would step back to a new erase pulse 301. When the block is found fully erased, it is subjected to an over-erase verify operation 304, which may be accomplished using a read operation and column current check. The read operation and column current check are well known in the art and not discussed further.

[0029] If a read operation is performed and column current is not detected 305, a successful erase operation has been performed 309. At this point, the erase operation is completed.

[0030] If a read operation is performed and column current is detected 305, the memory block has been over-erased and the high efficiency recovery operation 307, as described previously, is performed. The over-erase verify 304, column current detection 305, and high efficiency recovery 307 steps are then repeated until a successful erase operation has been detected by the lack of column current.

[0031] The erase operations of the present invention rely on high efficiency programming at low gate voltages attributed to secondary ionization phenomena. With the higher efficiency programming at lower cell current, more cells can be simultaneously programmed. For example, if programming takes 1 ms or less at a cell current of 100 nA or

less, all cells in a memory block can be recovered from the over-erased state in a relatively short time of 10 ms or less.

[0032] Figure 4 illustrates a block diagram of an electronic system in which an NROM array is embedded. This system is comprised of a microprocessor 401 and the NROM array 402. These components 401 and 402 are incorporated onto a single integrated circuit die. Alternate embodiments may add additional components such as input/output circuitry and other types of memory.

CONCLUSION

[0033] The methods of the present invention for erasing a short-channel, NROM memory block allow stable operation for the memory block over program/erase cycling. By ramping the control gate voltage, the threshold voltage for the memory block cells is allowed to increase at a constant rate that is equal to the rate of the voltage ramp. This ensures that the cell current is constant, low, and approximately equal for all cells in the block. Additionally, the threshold voltage for all of the cells at the end of the recovery operation does not exceed the maximum voltage at the end of the ramped voltage.

[0034] Although specific embodiments have been illustrated and described herein, it will be appreciated by those of ordinary skill in the art that any arrangement that is calculated to achieve the same purpose may be substituted for the specific embodiments shown. Many adaptations of the invention will be apparent to those of ordinary skill in the art. Accordingly, this application is intended to cover any adaptations or variations of the invention. It is manifestly intended that this invention be limited only by the following claims and equivalents thereof.